In the Drawings:

Please substitute Figure 2B with the replacement drawing, which has the "memory cell row 132" labeled properly.

REMARKS

Present Status of Patent Application

This is a full and timely response to the outstanding non-final Office Action mailed on August 24, 2005. The Examiner objected to the drawings for not including element 132, which was defined as a "memory cell row" in paragraph 36 of the specification. *See* Office Action at Page 2. The Examiner also objected to the specification and independent claim 1 for various informalities. *See id.* at Pages 2-3. Claims 2 and 7 were rejected also under 35 U.S.C. 112 as being indefinite for failing to particularly point out and distinctly claim the subject matter. *See id* at Pages 3-4. The Examiner further rejected claims 1-6 and 8-10 under 35 U.S.C. 102(e) as being anticipated by Hsieh (USP 6,645,813) and claim 7 under 35 U.S.C. 102(b) as being anticipated by Chang (USP 5,969,383). *See id.* at Pages 5-9. Finally, the Examiner rejected claim 8 under 37 C.F.R. 1.75 as being a substantial duplicate of claim 3. *See id.* at Page 9.

Upon entry of the amendments in this response, claims 1-10 and new claims 19-23 are pending in the present application. More specifically, claims 1, 2, 7-10 have been amended and claims 19-22 added. *See infra* at Pages 5-6. Claims 8-10 have been amended to become dependent on claim 7 instead of claim 1. *Id.* New claim 19 is a dependent claim of claim 1 while new claims 20-22 are dependent on claim 7. *Id.* It is believed that these amendments and additions add no new matter to the present application.

New Claims

Claims 19-22 have been newly added to further define and clarify the scope of the invention. The support for each claim is found in the current Specification as listed in the following table:

Claim #	Specification Source
19	Para. 33
20	Para. 33
21	Para. 33
22	Para. 35

New claims are dependent on either independent claim 1 or 7. Therefore, Applicant believes that new claims 19-22 are allowable over the prior art of record, given the reasons below that show why independent claims 1 and 7 are allowable. No new matter is believed to be added.

Response to Objections Based on Drawings

The Examiner has objected to the drawings because of the failure to label the "memory cell row." In response, Applicants have amended Figure 2B to show the element. Amended Replacement Sheet is also attached to this response. Withdrawal of the objection is therefore respectfully requested.

Response to Objections to Specifications

The Examiner objected to the specification for grammar informalities. In response, paragraphs 11 and 37 have been amended in accordance with the Examiner's comments. *See*

infra at Page 2. Applicants believe that these amendments enable the objections to be traversed.

Response to Objections to Claim Based on Informalities

According to the Office Action, claim 1 previously contained an error on line 3. *See* Office Action at Page 2. The claim has since been amended so that the second occurrence of the word "substrate" in line 3 has been replaced with the word "gate." It is believed that the foregoing amendments add no new matter to the present application. Applicants believe that these amendments place the claims in condition for allowance. Reconsideration and allowance of the application and presently pending claims are respectfully requested.

Response to Objections Under 35 U.S.C. Section 112

Claims 2 and 7 were rejected for failing to particularly point out the subject matter of the invention. *See* Office Action at Pages 3-4. Claim 2 has been amended in accordance with the Examiner's suggestion to clarify that the spacers are formed adjacent to and on both sides of each gate structure and each select gate structure so that no space exists within the memory cell row. *See infra* at Page 5. Independent claim 7 has also been amended in accordance with the Examiner's recommendation to qualify the source region as being disposed "in the substrate on one side of the gate structure opposite the select gate." *See id.* at Pages 5-6. Applicants wish to clarify that foregoing amendments of claims 2 and 7 have been made for purposes of better defining the invention in response to the rejections made under 35 U.S.C. §

112, and not in response to the rejections made based on prior art. Applicants believe that these amendments place the claims in condition for allowance. Reconsideration and allowance of the application and presently pending claims are respectfully requested.

Response to Objections Under 35 U.S.C. Section 102(e)

Claims 1-6 and 8-10 were rejected under 35 U.S.C. 102(e) as being anticipated by Hsieh (USP 6,645,824). *See* Office Action at Pages 5-8. Although Hsieh teaches a non-volatile memory structure comprising a plurality of gate structures and select gate structures, significant differences exist between Hsieh and the present invention so that a person of ordinary skill in the art could not anticipate the present invention from Hsieh. For at least the reasons stated below, Applicants respectfully assert that Hsieh does not anticipate the present invention because it fails to disclose all elements of the claims.

First, Hsieh teaches a gate structure that contains, from bottom to top, an oxide layer (110), a floating gate (120), an oxynitride film also known as ONO (130), a control gate (140), a silicon nitride layer (150) and a 4th polysilicon layer (220). *See* Hsieh, Col. 7, Lines 3-49; Col. 8, Lines 27-40 and Figs. 5e and 5f. More specifically, the ONO film contains a layer of bottom oxide layer, a middle layer of silicon nitride, and a top oxide layer. *See* Hsieh, Col. 7, Lines 14-20. In contrast, the present invention teaches a gate structure that contains, from bottom to top, a bottom dielectric layer, a charge-trapping layer made of silicon nitride, an upper dielectric layer, a control gate, and a cap layer. *See* Specification, Paras. 31-37 and Fig. 2B. The two gate structures differ in at least the following ways: Hsieh's silicon nitride layer

is embedded within the ONO film, which is located between the floating gate (FG) and the control gate (CG). *See* Hsieh, Figure 5e. The present invention, however, teaches a charge-trapping layer made from silicon nitride to be placed between the upper dielectric and bottom dielectric layers, essentially replacing the FGs in prior art and in Hsieh. *See* Specification, Figure 2B. Also, Hsieh's FG is made out of polysilicon while the present invention teaches a charge-trapping layer made out of silicon nitride. *Compare* Hsieh, Col. 7, Lines 3-14 *with* Specification, Para.33. Therefore, a person of ordinary skill in the art would not depart from Hsieh's teaching and replace the polysilicon FG with a silicon nitride layer.

In addition, Hsieh teaches that the fourth polysilicon layer (220), patterned to define select gates, serves as the word line that is oriented perpendicular to the first and second bit lines. *See* Hsieh, Col. 8, Lines 33-35. In contrast, the present invention teaches that the CG line should serve as the word line and also teaches the control gate line to be oriented in parallel to the SG lines (bit lines). *See* Specification, Paras. 33-40 and Fig. 3. Therefore, Hsieh does not anticipate claim 1, and the rejection should be withdrawn.

If independent claim 1 is allowable over the prior art of record, then its dependent claims 2-6 and 19 are allowable as a matter of law, because these dependent claims contain all elements of their respective independent claim 1. Therefore, reconsideration and allowance of the pending claims are requested.

Response to Objections Under 35 U.S.C. Section 102(b)

Claim 7 was rejected under 35 U.S.C. 102(b) as being anticipated by Chang (USP 5,969,383). *See* Office Action at Pages 8-9. Claim 7 has been amended to specify the thickness of the bottom dielectric layer of the gate structure to be between 20Å and 30Å. *See infra* at Page 6. This addition is supported by the specification. *See* Specification, Para. 35. Although Chang teaches a similar non-volatile memory structure as iterated in claim 7, Chang teaches that the top and the bottom dielectric layers should have thicknesses between 5nm and 15nm (or between 50Å and 150Å). *See* Chang, Col. 2, Lines 61-64; Col. 3, Lines 9-12. Since Chang teaches that the dielectric layers should be thick to have a good data retention rate, one of ordinary skill in the art would not depart from Chang's teaching to reach the present invention. *See* Chang, Col. 3, Lines 23-25. Dependent claims 20-22 further illustrate the thickness differences between the present invention and Chang's teachings. *See infra* at Page 6. For these reasons, Applicants respectfully assert that Chang is insufficient in anticipating claims 7 and its dependent claims 8-10 and 20-22. Applicants therefore request reconsideration and withdrawal of this objection.

Response to Objections of Double Patenting

The Examiner advised that should claim 3 be found allowable, claim 8 would be objected for being a substantial duplicate thereof. This objection was based on the previous form of claim 8, which was erroneously written as a dependent claim of claim 1 instead of claim 7. In line with Applicants' intention, claims 8-10 have all been amended to be

dependent on claim 7. Therefore, this objection should be traversed despite the allowance of claim 3. Applicants believe that no new matter has been introduced by these amendments and that all objections have been overcome. Favorable consideration and allowance of the present application and all pending claims are hereby courteously requested.

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CONCLUSION

For at least the foregoing reasons, it is believed that the presently pending claims 1-10, 19-22 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,

Date : Nov. 24, 2005

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